Quo Vadis, ISA & Cui Bono?

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Instruction set extensions are proliferating with every new CPU generation. While in the last decade most extensions concentrated on providing improved vector operation performance, e.g., for gaming and multimedia applications, a new trend is now evolving. With the introduction of the Haswell series of CPUs, Intel introduced their first version of Hardware Transactional Memory (HTM) as TSX-M instruction set extensions. Upcoming processor generations will support additional features, such as Memory Protection Extensions (MPX).

In this talk, I will give an overview of the current and expected functionality these extensions offer. Starting with an overview of the history of special-function instructions and an interesting detail from the RISC-vs-CISC debate of the early 1980's, the talk will then discuss details of the ISA extensions that have currently become available in current Intel CPUs as well as recently announced upcoming features.

In addition to giving an overview of useful features for implementing system software functionality, the talk will concentrate on advanced features of Transactional Memory and Memory Protection functionality described in recent operating system research literature and discuss the capabilities and limitations of the ISA extension implementations in current Intel CPUs for implementing this functionality.