Abstract

ReconOS: Multithreaded Programming for Reconfigurable Systems on Chip

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The rising density and heterogeneity of field-programmable gate arrays (FPGAs) enable the implementation of complete reconfigurable systems on a single chip. While such reconfigurable systems on chip integrate processor cores, reconfigurable logic cores, fixed-function cores, memories and interconnects, there is a lack of efficient programming models. Especially reconfigurable logic cores and the feature of partial hardware reconfiguration are not yet sufficiently supported by design methodologies and tools.

In this talk we present ReconOS, an ongoing project that aims at providing a programming model and execution environment for reconfigurable systems on chip. ReconOS bases on the open source operating systems eCos and Linux, and extends the widely-used multithreading programming model across the software/hardware boundary. First, we discuss the novel concept of hardware threads and show their interaction with the operating system. Then, we turn to the ReconOS execution environment which utilizes Xilinx Virtex FPGA technology and facilitates partial hardware reconfiguration. Finally, we report on a case study using software/hardware migration.